## IN THE CLAIMS

1. (Original) A memory device, comprising:

a NOR architecture NROM memory array formed on a substrate having a plurality of pillars and associated intervening trenches; and

a plurality of memory cell structures, each memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a first source/drain region formed at the bottom of the trench.

2. (Original) The memory device of claim 1, further comprising:

a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of memory cell structures;

at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

at least one second bit line, wherein the at least one second bit line is coupled to one or more second source/drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

3. (Original) The memory device of claim 2, wherein the plurality of memory cell structures are formed into rows and columns such that each trench contains a cell structure and where the NROM memory cell and select gate of each memory cell structures of each row are arranged in an alternating pattern, such that each pillar of the row has either two select gates or two NROM memory cells formed on opposing sidewalls.

4. (Currently Amended) An NROM memory cell structure, comprising:

a substrate, comprising two raised areas, defining a trench therebetween;

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of the trench;

a select gate ~~memory cell~~, wherein the select gate is formed vertically on a second sidewall of the trench; [[and]]

wherein the NROM memory cell is coupled to the select gate by source/drain regions at the bottom of the trench;

a word line, wherein the word line is coupled to a control gate of the NROM memory cell of the NROM memory cell structure;

a select line, wherein the select line is coupled to a control gate of the select gate of the NROM memory cell structure;

a first bitline, wherein the first bitline is coupled to a source/drain of the select gate; and

a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell.

5. (Original) The NROM memory cell structure of claim 4, wherein the raised areas are pillars.

6. (Currently Amended) The NROM memory cell structure of claim 4, wherein the second bitline is a source line ~~further comprising:~~

~~a word line, wherein the word line is coupled to a control gate of the NROM memory cell of the NROM memory cell structure;~~

~~a select line, wherein the select line is coupled to a control gate of the select gate of the NROM memory cell structure;~~

~~a first bitline, wherein the first bitline is coupled to a drain of the select gate; and~~

~~a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell~~.

7. (Currently Amended) An NROM memory array, comprising:

a substrate, comprising a plurality of pillars and associated intervening trenches; [[and]]

a plurality of memory cell structures, each memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench;

a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of memory cell structures;

at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures; and

at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of memory cell structures.

8. (Currently Amended) The NROM memory array of claim 7, wherein the second bitline is a source line ~~further comprising:~~

~~a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of NROM memory cell structures;~~

~~a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of NROM memory cell structures;~~

~~at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and~~

~~at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures~~.

9. (Currently Amended) The NROM memory array of claim 7 ~~claim 8~~, wherein the plurality of NROM memory cell structures are formed into rows and columns such that each trench contains an NROM memory cell structure and where the NROM memory cell and select gate of each NROM memory cell structure of each row is arranged in an alternating pattern, such that each pillar of the row has either two select gates or two NROM memory cells formed on opposing sidewalls.

10. (Original) The NROM memory array of claim 7, wherein the plurality of NROM memory cell structures are formed into rows and columns and an isolation region is formed between adjacent rows of NROM memory cell structures.

11. (Original) The NROM memory array of claim 10, wherein the isolation region is an oxide insulator.

12. (Original) The NROM memory array of claim 7, wherein the plurality of NROM memory cell structures are formed into rows and columns and each row of NROM memory cell structures is formed on a separate P-well isolation region formed on the substrate.

13. (Currently Amended) A memory device comprising:

a NOR architecture NROM memory array formed on a substrate having a plurality of pillars and associated intervening trenches;

a plurality of NROM memory cell structures, each NROM memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench;

a control circuit;

a row decoder;

a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of NROM memory cell structures;

a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of NROM memory cell structures;

at least one first bit/data line, wherein the at least one first bit/data line is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

at least one second bit/data line, wherein the at least one bit/data line is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures.

14. (Original) A system, comprising:

a processor coupled to at least one memory device, wherein the at least one memory device comprises,

a NOR architecture NROM memory array formed on a substrate having a plurality of pillars and associated intervening trenches, and

a plurality of NROM memory cell structures, each NROM memory cell structure comprising,

an NROM memory cell, wherein the NROM memory cell is formed vertically on a first sidewall of a trench, and

a select gate, wherein the select gate is formed on a second sidewall of the trench and wherein the select gate is coupled to the NROM memory cell by a source/drain region formed at the bottom of the trench.

15. (Currently Amended) A method of forming an NROM memory cell structure, comprising:

forming two raised areas on a substrate, the raised areas defining an associated intervening trench;

forming an NROM memory cell on a first sidewall of the trench;

forming a select gate on a second sidewall of the trench; [[and]]

forming a source/drain region at the bottom of the associated intervening trench;

forming source/drain regions on the top of the two raised areas;

forming a word line, wherein the word line is coupled to a control gate of the NROM memory cell of the NROM memory cell structure;

forming a select line, wherein the select line is coupled to a control gate of the select gate of the NROM memory cell structure;

forming a first bitline, wherein the first bitline is coupled to a source/drain of the select gate; and

forming a second bitline, wherein the second bitline is coupled to a source/drain of the NROM memory cell.

16. (Original) The method of claim 15, wherein forming two raised areas on a substrate further comprises etching a trench in the substrate.

17. (Original) The method of claim 15, wherein forming two raised areas on a substrate further comprises forming two pillars on a substrate.

18. (Original) The method of claim 17, wherein forming two pillars on a substrate further comprises depositing additional substrate material on the substrate to form the two pillars.

19. (Currently Amended) The method of claim 15, wherein forming a source/drain region at the bottom of the associated intervening trench and forming source/drain regions on the top of the two raised areas further comprises forming source/drain regions on the top of the two raised areas and at the bottom of the associated intervening trench in one of before the formation of the NROM memory cell and select gate and after the formation of the NROM memory cell and select gate.

20. (Original) The method of claim 15, wherein the substrate is P-doped.

21. (Original) The method of claim 15, wherein forming an NROM memory cell on a first sidewall of the trench and forming a select gate on a second sidewall of the trench further comprises forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall.

22. (Original) The method of claim 21, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall further comprises forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator.

23. (Original) The method of claim 21, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall further comprises forming an NROM transistor gate-insulator stack of one of oxide-nitride-oxide (ONO), oxide-nitride-aluminum oxide,

oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

24. (Original) The method of claim 22, wherein forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a trapping layer on the tunnel insulator, then forming the first and second insulators over the trapping layer and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the two raised areas and trench, masked, and directionally etched.

25. (Currently Amended) A method of forming a floating gate memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate by depositing a layer of masking material, patterning the masking material, and anisotropically etching the substrate; [[and]]

forming a plurality of NROM memory cell structures, each NROM memory cell structure having a trapping layer and a coupled select gate, where each NROM memory cell structure is formed by,

depositing a layer of tunnel insulator material over two pillars and an intervening trench;

masking and anisotropically etching the layer of tunnel insulator material to form a tunnel insulator of an NROM memory cell on a first sidewall of the trench;

depositing a layer of trapping layer material over the two pillars and intervening trench;

masking and anisotropically etching the layer of trapping layer material to form a trapping layer on the tunnel insulator on the first sidewall of the trench;

depositing a layer of gate insulator material over the two pillars and intervening trench;

masking and anisotropically etching the layer of gate insulator material to form a first gate insulator on the trapping layer on the first sidewall and a second gate insulator of a select gate on a second sidewall of the trench;

depositing a layer of gate material over the two pillars and intervening trench;

masking and anisotropically etching the layer of gate material to form a first and second control gates on the first and second gate insulators on the first and second sidewalls of the trench; and

diffusing a dopant material into the bottom of the trench and the tops of the two pillars to form source/drain regions of the select gate and the NROM memory cell;

forming a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of NROM memory cell structures;

forming a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of NROM memory cell structures;

forming at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

forming at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures.

26. (Original) The method of claim 25, further comprising:

forming the plurality of NROM memory cell structures into rows; and

forming an isolation region between adjacent rows of NROM memory cell structures by depositing an oxide insulator between adjacent rows.

27. (Currently Amended) A method of forming an NROM memory array, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate; and

forming a plurality of NROM memory cell structures, each NROM memory cell structure is formed by,

forming an NROM memory cell on a first sidewall of a trench;

forming a select gate on a second sidewall of the trench; and

forming a source/drain region at the bottom of the trench;

forming at least one first bit/data line, wherein the at least one first bit/data line is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

forming at least one second bit/data line, wherein the at least one second bit/data line is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures.

28. (Original) The method of claim 27, wherein the substrate is P-doped.

29. (Original) The method of claim 27, further comprising:

forming the plurality of NROM memory cell structures into rows; and

forming a P-well isolation region under each row of NROM memory cell structures.

30. (Original) The method of claim 27, further comprising:

forming the plurality of NROM memory cell structures into rows; and

forming an isolation region between adjacent rows of NROM memory cell structures.

31. (Original) The method of claim 30, wherein forming an isolation region between adjacent rows of vertical NOR architecture NROM memory cell structures further comprises forming an isolation region of an oxide insulator.

32. (Original) The method of claim 30, further comprising:

forming a plurality of word lines across the isolation region between adjacent rows of NROM memory cell structures, wherein each word line is coupled to a control gate of a single NROM memory cell of each row of NROM memory cell structures.

33. (Original) The method of claim 30, further comprising:

forming a plurality of select lines across the isolation region between adjacent rows of NROM memory cell structures, wherein each select line is coupled to a control gate of a single select gate of each row of NROM memory cell structures.

34. (Original) The method of claim 27, wherein forming an NROM memory cell on a first sidewall of the trench and forming a select gate on a second sidewall of the trench further comprises forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall.

35. (Original) The method of claim 34, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall further comprises forming an NROM transistor gate-insulator stack of one of oxide-nitride-oxide (ONO), oxide-nitride-aluminum oxide, oxide-aluminum oxide-oxide, oxide-silicon oxycarbide-oxide, composite layers of an oxide-an oxide of Ti, Ta, Hf, Zr, or La, and an oxide, composite layers of an oxide-a non-stoichiometric oxide of Si, N, Al, Ti, Ta, Hf, Zr, and La, and an oxide, composite layers of an oxide-a wet oxide not annealed, and an oxide, composite layers of an oxide-a silicon rich oxide, and an oxide, composite layers of an oxide-a silicon rich aluminum oxide, and an oxide, and composite layers of an oxide-a silicon oxide with silicon carbide nanoparticles, and an oxide.

36. (Original) The method of claim 34, wherein forming an NROM transistor gate-insulator stack on a surface of the first sidewall and forming a select gate transistor gate-insulator stack on a surface of the second sidewall further comprises forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and forming a second control gate over the second insulator.

37. (Original) The method of claim 36, wherein forming a tunnel insulator on the surface of the first sidewall, forming a trapping layer on the tunnel insulator, forming a first insulator as an intergate insulator over the trapping layer, and forming a first control gate over the first insulator, and on the surface of the second sidewall forming a second insulator and

forming a second control gate over the second insulator further comprises first forming a tunnel insulator on the surface of the first sidewall and forming a trapping layer on the tunnel insulator, then forming the first and second insulators over the trapping layer and on the surface of the second sidewall, and forming the first and second control gates over the first and second insulators, wherein each layer is deposited over the trench, masked, and directionally etched in combined layers to produce the NROM and select gate gate-insulator stacks.

38. (Currently Amended) The method of claim 27, wherein the at least one second bitline is a source line ~~further comprising:~~

~~forming at least one first bit/data line, wherein the at least one first bit/data line is coupled to one or more select gate drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and~~

~~forming at least one second bit/data line, wherein the at least one second bit/data line is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures~~.

39. (Original) The method of claim 27, wherein forming a plurality of NROM memory cell structures further comprises forming a plurality of NROM memory cell structures, wherein the plurality of NROM memory cell structures are formed into rows and where the NROM memory cell and select gate of each NROM memory cell structure of each row is formed in an alternating pattern, such that each pillar of the row has either two select gates or two NROM memory cells formed on its sidewalls.

40. (Currently Amended) A method of forming an NROM EEPROM memory device, comprising:

forming a plurality of pillars and associated intervening trenches on a substrate;

forming a plurality of NROM memory cells on a first sidewall of each trench;

forming a plurality of select gates on a second sidewall of each trench; [[and]]

forming one or more source/drain regions on the top of the plurality of pillars and at the bottom of the associated intervening trenches;

forming a plurality of word lines, wherein each word line is coupled to one or more control gates of the NROM memory cells of the plurality of NROM memory cell structures;

forming a plurality of select lines, wherein each select line is coupled to one or more control gates of the select gates of the plurality of NROM memory cell structures;

forming at least one first bitline, wherein the at least one first bitline is coupled to one or more select gate source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures; and

forming at least one second bitline, wherein the at least one second bitline is coupled to one or more NROM memory cell source/drain regions formed at the top of the plurality of pillars of the plurality of NROM memory cell structures.

41. – 71. (Canceled)